

IN THE TITLE:

Please delete the title as submitted and replace it as follows:

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME  
UTILIZING PERMITTIVITY OF AN INSULATING LAYER TO PROVIDE A  
DESIRED CROSS CONDUCTIVE LAYER CAPACITANCE PROPERTY

IN THE SPECIFICATION:

Replace the paragraph on page 6, starting at line 19, with the following rewritten paragraph:

Q1

Preferably, said first conductive layer is formed in a comb shape and said through-holes are formed at the positions sandwiched between the teeth of the comb.

Replace the paragraph on page 19, starting at line 7, with the following rewritten paragraph:

Q2

Prior to explaining the modes of carrying out a semiconductor device and a method of manufacturing it according to the invention, consideration is taken on a change in the element structure (structure in the wiring layer or polysilicon layer) due to downsizing of the process technique. Figs. 2 and 3 are views for explaining the element structure constituting the corresponding portion of a semiconductor integrated circuit (polysilicon gate nMOS transistor). Fig. 3 shows the element structure by more advanced downsizing of the process than the case of Fig. 2. Fig. 2(a) and Fig. 3(a) are plan views (pattern views); Fig. 2(b) and Fig. 3(b) are sectional views taken in line A-A' in Fig. 2(a) and Fig. 3(a), respectively, and Fig. 2(c) and Fig. 3(c) are sectional views taken in line B-B' in Fig. 2(a) and Fig. 2(c), respectively.

Replace the paragraph on page 24, starting at line 18, with the following rewritten paragraph:

A3 Further, the insulating inter-layer film can be made of a film having a high permittivity and the insulating inter-wiring film can be made of a film having a low permittivity. Thereby the capacitance between the through-holes and the capacitance between the wirings can be equalized. Further by laminating a plurality of films having different film quality from each other, better dielectric characteristics can be obtained.

Replace the paragraph on page 26, starting at line 4, with the following rewritten paragraph:

A4 The through-holes B11 and B12 generally have a fixed square shape in section as shown in Fig. 1(a). However, where a supplemental capacitor is formed, since through-holes are formed on a semiconductor substrate, an insulating layer thereon or an insulating substrate, the problem such as fluctuation of etching does not occur. Therefore, the rule of the fixed shape of the through-hole may be disregarded so that the through-holes has a rectangular shape in section as shown in Fig. 1(c). Thereby an area of capacitor is increased and a large capacitance can be obtained. And by use of capacitance along a through hole depth direction, such a large capacitance can be obtained without increasing an occupied area.

Replace the paragraph on page 29, starting at line 4, with the following rewritten paragraph:

A5 Contrary that, in Fig.4(c), although the through-hole B43 being contacted with the poly-Si P41 has regular square form wiring, the through-holes B41, B42 used for forming capacitors have a rectangular cross sections so as to increase an area facing to the poly-Si P41.

Replace the paragraph on page 39, starting at line 19, with the following rewritten paragraph:

a6 In Fig. 8, the poly-Si layer P81 has a planar shape formed along the respective side of an octagon so as to surround the through-hole B1. In the case that the poly-Si layer P81 has a regular square shape, a distance between the poly-Si layer P81 and the through-hole B81 at each edge portion of the regular square. Therefore according to the octagon shape, each edge portion of the regular square is made close to the through-hole B81. This shape can be realized in only a process rule in which the wiring of 45 degree on the skew of the right and left side is permitted. Where the wiring on the skew is not permitted, the planar shape of the poly-Si layer of P81 may be modified into the shape formed along the respective sides of a square. The planar shape of the poly-Si layer may be not the shape surrounding all the directions of the through-hole B81, but the shape partially surrounding the through-hole B81, e.g. an open-sided shape. In this case, it is also preferable that inner edge of the poly-Si layer P81 is formed along the outer side of the though hole.

Replace the paragraph on page 40, starting at line 23, with the following rewritten paragraph:

a7 Moreover, in this embodiment, the various patterns of poly-Si layer formed along the respective sides of an octagon and a square and open-sided shape may be registered as a single cell in a library of arranging/wiring tool (apparatus for assisting design of a semiconductor IC). Using these patterns alone or in combination, a supplemental capacitor having desired capacitance can be formed at a desired position. This can be applied to a semiconductor device with more regular arranging/wiring such as a gate array.

Replace the paragraph on page 41, starting at line 19, with the following rewritten paragraph:

a8 In Fig. 9, reference sign 901 denotes a Si substrate; B91m-B9jm and B91p-B9j+1p a through-hole; M92, M92 a metallic wiring; and P91-P9j+1 a poly-Si layer. The poly-Si layers P91-P9j+1 are connected to one another by the poly-Si layer shown in Fig. 9(a) under the metallic wiring M92. A spacer 911 is formed on the side of each poly-Si layer and its side face and upper face are covered with an insulating protection film 912. Although not shown in Fig. 9(b), an insulating inter-layer film is formed around each of the through-holes B91m-B9jm.

Replace the paragraph on page 42, starting at line 14, with the following rewritten paragraph:

a9 In Fig. 9, although the through-holes B91m-B9jm and poly-Si layer P91-P9j+1 were formed on the Si substrate 901, they may be formed on the insulating layer such an element isolation region of the Si substrate 901. Moreover, using an insulating substrate in place of the silicon substrate 901, this embodiment of the invention can be applied to a SOI (Silicon On Insulator) structure. This embodiment can also be applied to not only the MOS device but also the other device.

Replace the paragraph on page 43, starting at line 9, with the following rewritten paragraph:

a10 In Fig. 9, each of the through-holes B91m-B9jm is partially surrounded (e.g. on at least three of four sides) by the poly-Si layer. However, the pattern of the capacitor according to the second embodiment may be successively arranged (i.e. there is no poly-Si under the metallic wiring M91 in Fig. 9). Moreover, in this embodiment, the various patterns of the poly-Si layer such as a three-sided partially surrounding shape and a two-sided partially surrounding shape

Q10 may be registered as a single cell in a library of arranging/wiring tool (apparatus for assisting design of a semiconductor IC). Using these patterns in successive combination, a supplemental capacitor having desired capacitance can be formed at a desired position. This can be applied to a semiconductor device with more regular arranging/wiring such as a gate array.

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Replace the paragraph on page 46, starting at line 12, with the following rewritten paragraph:

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Q4 The structure as shown in Fig. 7 can be manufactured in the same manner as in the second embodiment, and can be realized at least in the following process. First, in a step of forming an electrode layer, poly-Si layers P101, P102 are formed on a Si substrate 1001. Next, in a step of forming an insulating protective film, a spacer 1011 is formed on the side of each of the poly-Si layers P101, P102 and an insulating protective film 1012 is formed to cover it. In a step of forming an insulating inter-layer film, the insulating inter-layer is formed. In a step of forming a through-hole, the insulating inter-layer film is etched to form a through-holes B101, B102. Further, in a step of forming a wiring, metallic wirings M101 and M102 are formed on the through-holes B101 and B102. Since the poly-Si layers are formed with high processing accuracy, the supplemental capacitor having an accurate capacitance can be formed.

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